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10/631,098	07/31/2003	Steven H. Voldman	BUR9-1999-0193US2	7752

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EXAMINER	
NGUYEN, LONG T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 01/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/631,098	VOLDMAN, STEVEN H.	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14,15,17-20,22 and 24-36* is/are pending in the application.

4a) Of the above claim(s) *15,19,20 and 22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14,17,18 and 24-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 December 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This office action is responsive to the amendment filed on 12/22/04.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because in Figure 6, reference character "43" has been used to designate both n-channel and p-channel transistors, and reference "45" has been used to designate both gates of n-channel and p-channel transistors.

The drawings are also objected to because it appears that the gate of transistor 42 in Figures 4-6 connected to the ground reference is incorrect since the gate of an n-channel transistor connected to ground reference will turn the n-channel transistor off. It appears that the gate of transistor 42 in Figures 4-6 be connected to power supply Vdd. Also, in Figure 4, it is not clear whether Vss is the same as the ground reference since Figure 4 shows the source of transistor 42 connected to ground reference while the source of transistor 43 connected to Vss, and it appears that sources of transistors 42 and 43 should be connected to the same reference. Also, in Figure 7, it appears that "Vss" should be changed to --Vdd-- because the Vss will turns both transistors 60 off.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure

must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities:

In the Pre-Amendment filed on 7/31/03, the amended to the specification is objected to because it is not provided on a separate sheet of paper. Also, the "_____" should be changed to --U.S. Patent No. 6,628,159 B2--.

In the original specification filed on 7/31/03, on line 15 of page 15, "IvtI" should be changed to |Vt|.

Appropriate correction is required.

Claim Objections

4. Claims 26 and 31 are objected to because of the following informalities:

Claim 26, line 1, "p-channel" should be changed to --n-channel-- because the n-channel transistor refers to the first gate and the first body, and the first RC discriminator connected to the first gate (see claim 24).

Claim 26, line 5, "n-channel" should be changed to --p-channel-- because the p-channel transistor refers to the second gate and the second body, and the second RC discriminator connected to the second gate (see claim 24).

Claim 31, line 3, "floating" should be deleted because when the body is floating, then it cannot be controlled.

Claim 35, line 2, "resistor" should be changed to –resistive transistor—to avoid lacking antecedent basis (see line 5 of claim 31).

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 27 and 29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 27, the recitation "an overvoltage or overcurrent condition" on line is unclear antecedent basis since it is not clear whether it is the same or different with "an overvoltage or overcurrent condition" recited earlier (see line 2 of claim 27). Clarification and/or appropriate correction is required.

With respect to claim 29, the recitation "said first circuit control network and said second control network provide different reference voltages" is misdescriptive because it is inconsistent with the operation of the circuitry (Figure 6). It is seen in the operation of Figure 6 that the voltage at node 40 will be pass through both transistors 60 to the bodies of the n-channel

transistor and the p-channel transistor, and thus the first control network (transistor 60 connected to body of n-channel transistor) and the second control network (transistor 60 connected to body of p-channel transistor) will have the same voltage as the voltage at node 40; and cannot have provide different reference voltages. Clarification and/or appropriate correction is required.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 14 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Au et al. (USP 5,528,188) in view of Brady et al. (USP 5,314,841).

With respect to claims 14 and 17, Figure 4b of the Au et al. reference discloses a device which includes: a MOSFET transistor (Q1) comprising a gate (gate of Q1), a body (body of Q1); an RC discriminator circuit (32) comprising a resistor (R) and a capacitor (C), and a circuit control network (40) modulating a potential of the body (of M) to provide ESD protection (the circuit of 40 capable of controlling the potential biasing the body of the transistor and therefore it also capable of provide ESD protection) . The Au et al. reference does not disclose that the circuit in Figure 4b is fabricated by using silicon-over-insulator SOI technology. However, the Brady et al. reference discloses that silicon-over-insulator (SOI) technology provides advantages over regular silicon technology such as increasing the operating speed and reducing the power consumption of the circuitry (Col. 1, lines 12-15). Therefore, it would have been obvious to one having an ordinary skill in the art at the time the invention was made to modify the circuit in

Figure 4b of the Au et al. reference by using specific SOI technology to fabricate the circuitry for the purpose of increasing the operating speed and reducing the power consumption of the circuitry. Thus, this modification meets all the limitation of claims 14 and 17. Note that, in the above modification, the functional limitation in claim 17 is also met as the operation of control network circuitry modulates the potential voltage of the body and limit the body to a reference voltage.

9. Claims 18 and 31-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Au et al. (USP 5,528,188) in view of Brady et al. (USP 5,314,841), as discussed in claim 14 above, and further in view of Sasaki (USP 5,039,873).

With respect to claims 31 and 32, the modification/combination of Au et al. and Brady et al. as discussed in claim 14 above meets all the limitations of this claim except that the resistor R is a resistive-transistor. However, the Sasaki reference teaches in Figure 4C that a MOSFET transistor is functionally equivalent to a resistor when the MOSFET transistor is ON (see Figure 4c, and Col. 1, lines 21-22 of Sasaki). Therefore, it would have been obvious to one having an ordinary skill in the art at the time the invention was made to modify the above circuitry by substitute an always ON MOSFET transistor (i.e., a MOSFET transistor having a DC bias at its gate so that the MOSFET transistor is ON) for each of the resistors in the circuitry because they are functionally equivalent and for the purpose that it is easily integrated. With such a modification, the limitation of claim 31 is met as that the RC discriminator including a resistive-transistor and a capacitor. Note that, in the above modification, the functional limitation in claim 32 is also met as the operation of control network circuitry modulates the potential voltage of the body and limit the body to a reference voltage. Also, note that the device includes a source S

and a drain D (Figure 4b of Au et al.), wherein the source is connected to the resistive-transistor (both connected to ground), and the drain is connected to the capacitor as recited in claim 34; and the functional limitation that the resistor (resistive transistor) and said capacitor initiate coupling of the gate the an over-voltage or over-current condition exits (recited in claim 35) is also met (Col. 5, lines 30-67 of Au et al.) and also because the structure of the RC discriminator connected to the gate of the MOSFET device of the Au et al. is substantially identical as the structure of the RC discriminator of the inventions. Also, Figure 4b of the Au et al. shows a PAD (PAD) coupled to the capacitor (for claim 36).

With respect to claims 18 and 33, the modification/combination as discussed in claim 31 meets the limitations of these claims that the circuit control network (40, Figure 4b of Au et al.) includes at least a SOI MOSFET because the circuitry is fabricate by using SOI technology (discussed in claim 14), and because every resistor in the circuitry is formed by using an always ON MOSFET transistor (as discussed in claim 31) so the SOI MOSFET in this claim is the always ON MOSFET transistors for resistors R1 and R2 in circuit 40 of Figure 4b.

10. Claims 24 and 26-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ker et al. (USP 5,631,793) in view of Au et al. (USP 5,528,188), and further in view of Brady et al. (USP 5,314,841).

With respect to claim 24, Figure 2 of the Ker reference discloses a device which includes: an n-channel MOSFET (Mn1) comprising a first body and a first gate; a p-channel MOSFET (Mp1) comprising a second body and a second age; a first RC discriminator (Rn, Cn1) comprising a first resistor (Rn) and a first capacitor (Cn1); and a second RC discriminator (Rp, Cp1) comprising a second resistor (Rp) and a second capacitor (Cp1). The Ker reference does

not discloses the device a first circuit control network for modulating a potential voltage of the first body, and a second circuit control network for modulating a potential voltage of the second body. However, the Au et al. reference discloses in Figure 6 a device that includes first and second circuit control networks (SCR 52 and 50, wherein the detail of the SCR is shown as circuit 40 in Figure 4b) for controlling the first and second bodies (bodies of Q3 and Q2), respectively for the purpose of improving the level of ESD protection of either a positive or negative polarity ESD event (see line 59 of Col. 5 to line 23 of Col. 6). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to provide the device of Figure 2 of the Ker et al. reference with the first and second circuit control networks connected to the first and second bodies, respectively, for the purpose of improving the level of ESD protection of either a positive or negative polarity ESD event. Thus, this modification meets the limitations of the first and second circuit control networks as recited in claim 24 including the functional limitation "to provide ESD protection".

The combination of the Ker et al. reference and the Au et al. reference meets all the limitations of claim 24 except that the circuitry is fabricated by using silicon-over-insulator SOI technology. However, the Brady et al. reference discloses that silicon-over-insulator (SOI) technology provides advantages over regular silicon technology such as increasing the operating speed and reducing the power consumption of the circuitry (Col. 1, lines 12-15 of Brady et al.). Therefore, it would have been obvious to one having an ordinary skill in the art at the time the invention was made to modify above combination by using specific SOI technology to fabricate the circuitry for the purpose of increasing the operating speed and reducing the power consumption of the circuitry. Thus, this modification meets all the limitation of claim 24.

With respect to claim 26, Figure 2 of the Ker et al. in the above combination shows the n-channel SOI MOSFET Mn1 comprises a source and a drain connected to the first resistor (Rn) and the first capacitor (Cn1); and the p-channel SOI MOSFET transistor includes a source and a drain connected to the second resistor (Rp) and the second capacitor (Cp1).

With respect to claim 27, the functional limitation that the first resistor and capacitor and the second resistor and capacitor initiate coupling of the first gate and the second gate, respectively, when an over-voltage or over-current condition exists is met (see line 65 of Col. 4 to line 5 of Col. 5). Further, because the structure of the first and second RC discriminator circuit connected to the first and second gates is substantially identical to applicant's invention so it must functions the same.

With respect to claim 28, it is seen in the operation of the combination/modification circuitry that the first circuit control network limits the first body to a reference voltage, and the second circuit control network limits the second body to the reference voltage (both of the circuit control networks SCR in the above combination/modification are the same so they must limit the same reference voltage).

Insofar as understood in claim 29, because of the two circuit control networks SCR in the above combination/modification are the same which are similar as applicant's invention (both the control networks are the same), so if two of the same control networks of applicant's invention meets the misdescriptive limitation "provide different reference voltages", then two of the same SCR (control networks) in the above combination/modification would also "provide different reference voltages".

With respect to claim 30, the above combination/modification circuitry shows a pad (21, Figure 2 of Ker et al.) connected between the n-channel and p-channel SOI MOSFETs.

11. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ker et al. (USP 5,631,793) in view of Au et al. (USP 5,528,188) and Brady et al. (USP 5,314,841), as discussed in claim 24, and further in view of Sasaki (USP 5,039,873).

With respect to claim 25, the modification/combination of Ker et al., Au et al. and Brady et al. as discussed in claim 24 above meets all the limitations of this claim except that first and second circuit control network comprises at least one SOI MOSFET. However, the Sasaki reference teaches in Figure 4C that a MOSFET transistor is functionally equivalent to a resistor when the MOSFET transistor is ON (see Figure 4c, and Col. 1, lines 21-22 of Sasaki). Therefore, it would have been obvious to one having an ordinary skill in the art at the time the invention was made to modify the above combination/modification circuitry by substitute an always ON MOSFET transistor (i.e., a MOSFET transistor having a DC bias at its gate so that the MOSFET transistor is ON) for each of the resistors in the circuitry because they are functionally equivalent and for the purpose that it is easily integrated. With this modification, the limitations of this claim is met because the first and second circuit control networks (40, Figure 4b of Au et al.) includes at least a SOI MOSFET because the circuitry is fabricate by using SOI technology, and because every resistor in the circuitry is formed by using an always ON MOSFET transistor so the SOI MOSFET in this claim is the always ON MOSFET transistors (for resistors R1 and R2 in circuit 40 of Figure 4b of Au et al.).

Response to Arguments

12. Applicant's arguments filed on 12/22/04 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

January 26, 2005

Long Nguyen
Primary Examiner
Art Unit: 2816